Instantaneous Model of a MESFET for use in Linear and Nonlinear Circuit Simulations

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Abstract—**A formal approach for nonlinear modeling of FET's is presented. The intrinsic transistor is described by current and charge generators, that are instantaneously dependent on the two internal voltages. The extrinsic parasitic elements are also included. This instantaneous model is obtained from the small signal equivalent circuit computed at a number of bias points, by integration of the bias dependent elements. A program for using this model in nonlinear circuit analysis has been developed. The process has been carried out for two transistors, one being of low noise, and the other a power MESFET. Good agreement has been observed when comparing the nonlinear analysis with measured data. Finally a Solid State Power Amplifier at 28 GHz has been designed using the power transistor, delivering 21 dBm at 1 dB compression point.**

I. Introduction

SINCE most active microwave circuits contain nonlinear solid-state devices, such as MESFET's or HMET's, an accurate tool for predicting their nonlinear characteristics is required. The most common solution consists of modeling these transistors by a network of lumped time-invariant linear and nonlinear elements. Once this equivalent circuit has been obtained, the analysis and optimization of any subsystem (amplifier, mixer, oscillator, etcetera) containing the transistor can be made with the aid of common commercial software packages, such as LIBRA, SUPER COMPACT, HP-MDS · · · The results of any of these packages is questionable if the mathematical description of the transistor (equivalent circuit) does not predict accurately its actual behavior. Thus the key point of nonlinear simulation is the active device nonlinear characterization, which is a difficult and yet unresolved matter.

The nonlinear model of a transistor basically includes voltage dependent current generators and nonlinear capacitances. The predominant nonlinearity is that corresponding to the drain current (I_d) and is usually obtained by fitting the dc characteristics of the transistor to analytical formulas. Many papers have recently been published following this approach and proposing different approximations. Well-known are the papers from Tajima *et al* [1], Curtice *et al.* [2], Materka *et al.* [3], Statz *et al.* [4] and others. A good review of all these methods can be found in Chapter 2 of [5]. Also, many commercial nonlinear simulators include such expressions as standard nonlinear descriptions of transistors. As pointed out in [5], the dc characterization of a transistor is questionable if it is to be used at microwave or millimeter wave frequencies.

The nonlinear capacitances are also approximated by analytical expressions, for which there are also different suggestions from the same above mentioned authors. The most popular solution consists of using the known varactor capacitance expression for C_{gs} keeping the rest of the capacitances constant. Obtaining the curve-fitting parameters for the expressions of the capacitances of a given transistor cannot be accomplished in dc operation, and is difficult. Most authors, although they admit a nonlinear behavior of the capacitances, use the small signal values for the nonlinear analysis, arguing that the effect of considering such nonlinearities is small, the drain current being the most important effect.

The rest of the nonlinear equivalent circuit intrinsic elements are obtained by small signal analysis, fitting the measured and computed S-parameters in a large frequency band. Usually the optimization is carried out assuming constant values of the elements that can be computed by partial derivation of nonlinear data (for example g_m and G_{ds} from I_d).

This paper presents a different approach in nonlinear modeling. First, a new circuit topology for the instantaneous simulation of the transistor is proposed. It has essentially charge and current generators which depend on two voltages. This circuit is analyzed for small signal operation, thus obtaining a corresponding linear equivalent circuit, which is slightly different to the one usually found in the literature.

The element values for this small signal equivalent circuit are obtained by using dc and ac small signal measurements following a similar method of that described by Dambrine *et al.* [6]. It provides a fast and accurate determination of the value of all the elements based on S-parameters measured in a low frequency band ($f < 3$ GHz) and an additional dc-measurement. Further optimization is performed to improve the fitting to measured S parameters to 40 GHz. The procedure is carried out at different bias points, obtaining the variation of the elements with

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the bias voltages, as was already proposed by Willing *et al.* [7]. This data, however, is used in a different way. From them the charge and current genertors for the instantaneous model are obtained through a set of equations that relate the instantaneous circuit to the small-signal equivalent circuit. Thermal effects and frequency dispersion have not yet been included in the model.

The method has been tested on a GaAs low noise FET (Fujitsu's FSX02X) and on a power GaAs FET (Toshiba's JS8864-AS), with satisfactory results. Also a power amplifier at 28 GHz has been designed from data obtained for the last one. The output power agrees with the data supplied by the manufacturer.

The paper is organized as follows: Section II describes the theory and Section III is devoted to the small signal equivalent circuit parameter extraction method. The nonlinear analysis is discussed in Section IV, and Section V shows the results obtained with the two transistors tested and the power amplifier designed.

II. Theoretical Analysis

A. Instantaneous Model of a Transistor

The instantaneous model for a transistor, proposed previously in [8], is shown in Fig. 1. The two instantaneous current functions, $I_g(V_g, V_d)$ and $I_d(V_g, V_d)$ stand for the conduction phenomena, while the two instantaneous charge functions, $Q_g(V_g, V_d)$ and $Q_d(V_g, V_d)$, represent the charge stored in the transistor. Parasitic elements R_g, R_s, R_d, L_g, L_s, L_d, C_1, C_2 are assumed to be linear.

This model has few nonlinear elements, and simple topology. It is interesting to note that it has no explicit feedback branch between gate and drain, which greatly enhances the computing efficiency in nonlinear analysis. Since the instantaneous capacitance effects are described by charge functions, the nonlinear analysis by harmonic balance is simple and fast. The quasistatic approximation has been assumed, which means that I_g, I_d, Q_g and Q_d are functions of the instantaneous voltages v_g, and V_d at the same time instant. There is no explicit time delay in the dependence of the drain current with respect to the gate voltage. This makes the analysis easier for a computer program, because it does not have to deal with the prob-

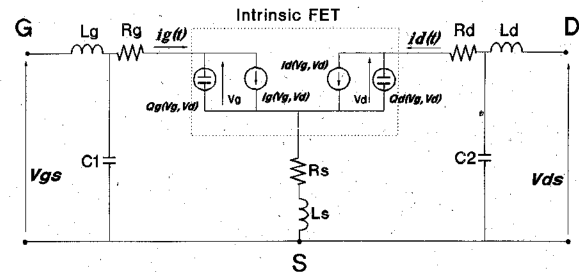


Fig. 1. Proposed instantaneous model of a MESFET including the external parasitic elements.

$$i_d(t) = I_d(V_g(t), V_d(t)) + \frac{d}{dt} Q_d(V_g(t), V_d(t)). \quad (2)$$

Assuming now a small signal operation, the time dependent voltages will be

$$V_g(t) = V_g + \text{Re}\,[V_{ga}e^{j\omega t}]$$
$$V_d(t) = V_d + \text{Re}\,[V_{da}e^{j\omega t}] \quad (3)$$

where V_g and V_d are the dc bias voltages, and V_{ga} and V_{da} the voltage complex phasors. Substituting (3) in (1), (2) and assuming a linear Taylor expansion of (1) and (2), the corresponding current phasors can be written:

$$i_{ga} = (G_{11} + j\omega C_{11})\, V_{ga} + (G_{12} + j\omega C_{12})\, V_{da} \quad (4)$$

$$i_{da} = (G_{21} + j\omega C_{21})\, V_{da} + (G_{22} + j\omega C_{22})\, V_{da} \quad (5)$$

where

$$G_{11} = \frac{\partial I_g}{\partial v_g}, \quad G_{12} = \frac{\partial I_g}{\partial v_d}, \quad G_{21} = \frac{\partial I_d}{\partial v_g}, \quad G_{22} = \frac{\partial I_d}{\partial v_d}$$

$$C_{11} = \frac{\partial Q_g}{\partial v_g}, \quad C_{12} = \frac{\partial Q_g}{\partial v_d}, \quad C_{21} = \frac{\partial Q_d}{\partial v_g}, \quad C_{22} = \frac{\partial Q_d}{\partial v_d} \quad (6)$$

being all the partial derivates computed at the bias point V_g and V_d. Equations (4) and (5) are the *Y*-parameter description of a network, and a "pi" topology can be used as an equivalent circuit. Fig. 2 shows this pi-network embedded in the parasitic elements of the FET. Identify-

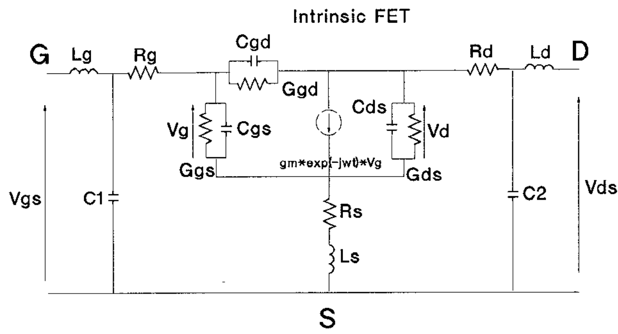


Fig. 2. Equivalent circuit for incremental small signal voltages. The elements are bias dependent.

TABLE 1
VALUES FOR THE ELEMENTS OF THE EQUIVALENT CIRCUIT OF TRANSISTOR FSX02X AS COMPUTED AND AFTER OPTIMIZATION

Name	Value		Name	Value	
	Before Optimiz.	After Optimiz.		Before Optimiz.	After Optimiz.
Rs (Ω)	1.6	2.7	*Cgd* (pF)	0.04	0.033
Rg (Ω)	3.7	4.1	*Cgs* (pF)	0.44	0.28
Rd (Ω)	2.7	1.93	*Cds* (pF)	0.15	0.082
Ls (nH)	0.045	0.023	*gm* (mS)	45.8	39.8
Lg (nH)	0.126	0.16	τ (ps)	0	3.09
Ld (nH)	0.2	0.17	*Ggs* (mS)	0	0
Gds (mS)	3.14	1.64	*Ggd* (mS)	0	0

current and charge functions at the bias point, as shown in (6).

C. Instantaneous Model from Small Signal Measurements

Integrating equations (6), the charge and current generators of the instantaneous model of Fig. 1 are obtained:

$$Q_g(V_g, V_d) = \int_0^{v_g} C_{11}(\xi, v_d)\, d\xi + \int_0^{v_d} C_{12}(0, \xi)\, d\xi + Q_g(0, 0) \quad (8)$$

$$Q_d(v_g, v_d) = \int_0^{v_g} C_{21}(\xi, v_d)\, d\xi + \int_0^{v_d} C_{22}(0, \xi)\, d\xi + Q_d(0, 0) \quad (9)$$

$$I_g(v_g, v_g) = \int_0^{v_g} G_{11}(\xi, \lambda_d)\, d\xi + \int_0^{v_d} G_{12}(0, \xi)\, d\xi + I_g(0, 0) \quad (10)$$

$$I_d(v_g, v_d) = \int_0^{v_g} G_{21}(\xi, v_d)\, d\xi + \int_0^{v_d} G_{22}(0, \xi)\, d\xi + I_d(0, 0) \quad (11)$$

where $I_g(0, 0) = I_d(0, 0) = 0$ and $Q_g(0, 0)$ and $Q_d(0, 0)$ are irrelevant integration constants. Alternative expressions can be found by changing the order in which the integrations are performed, but this makes little difference.

Thus from the evolution of C_{ij} and G_{ij} as functions of the bias voltages V_g, V_d one can compute the voltage dependent charge and current instantaneous functions $I_g(v_g, v_d)$, $I_d(v_g, v_d)$, $Q_g(v_g, v_d)$, and $Q_d(v_g, v_d)$. In turn C_{ij} and G_{ij} can be obtained from the elements of the small signal equivalent circuit using (7), which can be written in the following manner:

$$G_{11} = G_{gs} + G_{gd} \qquad G_{12} = -G_{gd}$$
$$C_{11} = C_{gs} + C_{gd} \qquad C_{12} = -C_{gd}$$
$$G_{21} = g_m \cos \omega\tau - G_{gd} \qquad G_{22} = G_{gd} + G_{ds}$$
$$C_{21} = -g_m \frac{\sin \omega\tau}{\omega} - C_{gd} \qquad C_{22} = C_{gd} + C_{ds}. \quad (12)$$

Finally, the values of the intrinsic elements of Fig. 2 for different gate and drain voltages can be obtained by measuring the *S*-parameters of the FET in a wide range of bias conditions, and extracting a small signal equivalent circuit at each bias point. Section III describes the method that has been used.

Notice that the small signal equivalent circuit of Fig. 2 is different from those usually found in the literature. The impedances from gate to source and gate to drain are a parallel combination of resistor and capacitance instead of a series combination of the same elements, as is usually considered. As will be shown in Section V, when one carries out this procedure for a real transistor, it happens that conductances G_{gs} and G_{gd} vanish, (see Table I) resulting in a circuit similar to the one normally used, except for the internal resistance R_I that here does not appear. Many authors also do not include this resistance for nonlinear simulations.

The current and charge generators of figure 1 are functions of the internal voltages v_g and v_d, but the data obtained from the *S*-parameter measurements at a number of bias points gives the variation of the elements with the external voltages V_{gs} and V_{ds} (Fig. 2). To change the variables, the circuit of Fig. 1 is analyzed in dc. Assuming that I_g is negligible compared with I_d:

$$V_{ds} = V_d + (R_d + R_s)\, I_d$$
$$V_{gs} = V_g + R_s\, I_d. \quad (13)$$

Now, measuring the dc output characteristics of the transistor, the dependance of I_d with V_{gs} and V_{ds} is obtained. When inserted in (13) the values of the internal voltages V_g and V_d can be readily obtained for each pair (V_{gs}, V_{ds}).

Intrinsic elements are then expressed as functions of the internal voltages V_g, V_d, and incremental capacitances and conductances are deduced from (12). With (8)-(11) the current and charge functions of the instantaneous model of the FET are computed.

III. Small Signal Parameter Extraction

The small signal equivalent circuit determination is the first step in obtaining the instantaneous model. It is very important to have and accurate procedure since all the data in the model is computed from this equivalent circuit. Much work has been devoted in the last years to small signal modelling and there are many approaches (see for example [9]). One of the more common procedures is by minimizing an error function which depends on the difference between the S-parameters of the equivalent circuit and those of the transistor, measured at a number of frequencies in a large bandwidth. All the elements of the equivalent circuit are varied until a minimum of the error function has been found. One of the main problems of this method is the determination of the starting values for the optimization procedure to start. Depending upon these starting values, the final ones may be very different, even with low error functions. Moreover, the extrinsic resistances often tend to vanish independently of their starting values, obtaining a result which lacks of physical meaning. Since, to obtain the variation of the intrinsic elements with the bias voltages, the procedure will have to be carried out many times keeping always constant the extrinsic elements, it is important that these ones have meaningful values, valid for all bias conditions.

A. Intrinsic Elements

The intrinsic part of the FET (Fig. 2) has 8 elements, and, as Dambrine *et al.* have suggested [6], they can be calculated analytically from its *Y*-parameters, which, in turn can be obtained from the *S*-parameters of the transistor, provided the extrinsic elements are known and deembedded. The problem has then been reduced to obtain the 8 extrinsic elements.

B. Extrinsic Elements

Several methods exist in the literature for obtaining the extrinsic elements, especially the resistances. Both dc and ac measurements have been suggested, but in almost all cases the transistor is biased at special conditions for which a very simple equivalent circuit is assumed (usually $v_{gs} > 0$ and $V_{ds} = 0$). In this equivalent circuit, which in its more general form is depicted in Fig. 3, the intrinsic FET operation is modelled by an ideal Schottky junction Z_d and, in some cases, a channel resistance R_c. For sufficiently low frequency, the parasitic capacitances C_1 and C_2 may be neglected and the inductances are obtained very easily from the slope of the imaginary part of the *Z*-parameters (obtained from low frequency *S*-parameter measurements) plotted against frequency [6].

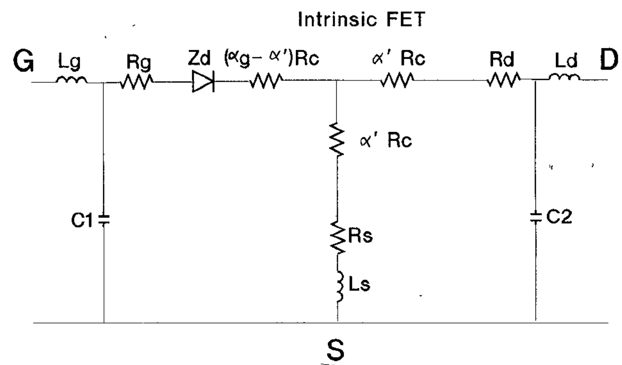


Fig. 3. Equivalent circuit of a FET for positive gate voltage and zero drain voltage. R_c is the channel resistance, and Z_d represents an ideal Schottky junction.

The resistances may be obtained by comparing dc or ac measurements, with the predictions of the model of Fig. 3. Two constants appear in it: α_g and α' which are given different values depending upon the author.

Many authors (for example [10], [11], and [5]) neglect the channel resistance, which is equivalent to making α_g and α' equal to zero in Fig. 3. Then three measurements are sufficient to obtain the three resistances. The mentioned references use dc measurements of the *I-V* characteristics corresponding to the FET with alternatively grounded the source, the drain and both terminals. In all these cases the circuit of Fig. 3 transforms into a schottky junction with a series resistance which can be easily obtained by comparison of the measured and predicted *I-V* characteristics. The same circuit is used in [12] for measuring $R_s - R_d$ and R_g once $R_s + R_d$ has been obtained from the $I_d - V_{ds}$ dc characteristics in the linear region. It is interesting to note that for that last measurement this author does takes into account the channel resistance, and uses an expression that relates it to the gate voltage.

Using the same values for α_g and α', data can also be obtained from the measurement of *S*-parameters at different gate current. The real parts of the circuit form Fig. 3 with $\alpha_g = \alpha' = 0$ are:

$$\begin{aligned} \text{Re}\,[Z_{11}] &= R_g + R_s + nKT\, qI_g \\ \text{Re}\,[Z_{12}] &= R_s \\ \text{Re}\,[Z_{22}] &= R_s + R_d. \end{aligned} \tag{14}$$

Thus, the extrapolation of Re $[Z_{11}]$ versus $1/Ig$ gives $R_g + R_s$ which, combined with the other two equations allows the determination of the three resistances. In any case, they are obtained with only three measurements, because the channel resistance has not been taken into account.

The second choice, proposed in [13] and used also in [6], considers $\alpha_g = 1/3$ and $\alpha' = 1/2$ for all gate bias conditions and $V_{ds} = 0$. In this case the channel resistance is an unknown, and an extra equation is needed. In [13] an expression relating R_c with the gate voltage is used, and in [6] an extra dc measurement is also proposed, this being for example that of $R_s + R_d$ suggested in [12]. In

both references the resistances are obtained from AC measurements.

The third choice is using the results of [14] in which these constants are expressed as functions of the gate current. They are obtained for the interpretation of 'end-resistance' measurements by computing the total dynamic resistance from gate to source assuming a floating drain terminal. For low gate currents, the values of α_g and α' are the same as those given above (namely $1/3$ and $1/2$ respectively) and for most practical cases these values can be used. However, according to [6], the capacitance effects of the Schottky junction can be neglected only if the gate current is large enough, which is in contradiction with the above statement. Finally note that these results are obtained for floating drain terminal, whereas they are often used for $V_{ds} = 0$, which is not the same condition.

The dependence of α_g and α' with I_g has been used in [15] for the determination of the resistances from ac measurements. In this paper, the extra equation needed to compute R_c is obtained from the measurement of the S-parameters with floating source terminal, which is difficult to make, especially for transistors having via holes.

Most of the methods outlined in the previous paragraphs were tested in our laboratory, giving serious discrepancies. Finally, it was decided to use those obtained from the method of [6] and [12] as starting values in an optimization process. The extrinsic elements were computed from low frequency S-parameters measurements (1 to 3 GHz) of the cold FET. From the measured S-parameters in the same frequency band at normal bias, the intrinsic ones were then analytically computed. Thus at each frequency point, from 1 to 3 GHz, a set of extrinsic and intrinsic element values was obtained. See Section V for experimental results.

C. Optimization

Although the elements were obtained from measurements to 3 GHz, the fitting between computed and measured S-parameters was good to 40 GHz. Nevertheless, to obtain a better agreement in the full band an optimization was necessary.

The S-parameters of the transistor at its nominal bias point from 6 GHz to 40 GHz were measured (see Section V) using TRL calibration. They were compared with those of the equivalent circuit obtained so far, optimizing its elements to minimize the error function between both sets. First only the intrinsic elements were allowed to vary, and in a second pass, keeping these ones fixed, the extrinsic elements were optimized.

Once the elements had been obtained at the nominal bias point, their values for other bias voltages were obtained only from optimization. For each bias point, the starting values were those obtained in the previous point. The intrinsic elements were kept constant, equal to the values obtained for the nominal bias.

All the optimizations have been carried out using a commercial program (MDS from Hewlett Packard). For the repeated optimization at different bias points the journaling option of the program has been used.

IV. Nonlinear Analysis

The model of Fig. 1 is very well suited for nonlinear analysis using Harmonic Balance since the nonlinear behavior is described by means of voltage controlled charge and current generators in the time domain. The extrinsic elements of the model are embedded in the linear circuit to be analyzed.

A. Interpolation

The procedure for modeling presented leads to instantaneous charge and current functions which depend on two voltages. These functions are obtained as a matrix of numbers giving their values at discrete voltage points, at which the measurements have been made. For the Harmonic Balance analysis the values at any voltage have to be known so some kind of interpolation has to be done. Furthermore, when the transistor is working in nonlinear operation, the instantaneous values of the drain and gate voltages may exceed (in fact, they do) the maximum allowable dc values. For dynamic nonlinear analysis, the transistor has to be characterized also to these extreme voltages for which no data can be supplied from measurements. In mathematical terms, this means that an extrapolation is necessary. In the following paragraphs the methods of obtaining analytical functions for the measured values of $I_g(V_g, V_d)$, $I_d(V_g, V_d)$, $Q_g(V_g, V_d)$ are discussed. This is also useful if the model is to be introduced in a commercial software for nonlinear analysis. A further advantage of using analytical functions is that the derivatives are known, and the jacobian can be computed very fast.

To guarantee the convergence of the simulation, the functions used in the interpolation have to be defined and be continuous to the first derivate for all the voltages used in the simulation. This is a very strong restriction, and, in particular, a local interpolation at each point from the values at the adjacent ones is not suggested since it leads to discontinuities in the derivative. It may give, however, satisfactory results for small to moderate signals.

A possible candidate for the interpolation could be a two dimensional polynomial of orders n_1 and n_2:

$$\begin{aligned} f(V_1, V_2) = {} & a_{00} + a_{01}V_1 + a_{10}V_2 + a_{11}V_1V_2 \\ & + a_{12}V_1V_2^2 + a_{21}V_1^2V_2 \\ & + \cdots + a_{n_1}\, a_{n_2}\, V_1^{n_1}V_2^{n_2} \end{aligned} \quad (15)$$

which meets all the requirements. The coefficients of this polynomial are computed by minimizing the rms error at all measured points. But, to have low error, its degree must be large, giving unwanted ripples in the interpolated data between two measured points. This method was discarded because these ripples generated nonlinearities

which did not exist, incrementing the number of harmonics and their amplitudes.

The method used in the present work consists of a separate interpolation of the two variables. Given a bias point V_{1Q}, V_{2Q}, a two-variable function can be approximated by two functions of single variable:

$$f(V_1, V_2) \approx A f(V_1, V_{2Q}) \cdot f(V_{1Q}, V_2)$$

being A a normalizing constant. Each function of one variable can then be interpolated separately. This approach has the advantage that, even with simple interpolation functions, the solution will always be accurate in the bias point. For large amplitude excursions from the bias point, at the extreme voltage values, the accuracy may be poorer, but this has been observed to be a secondary effect not affecting the global accuracy of the solution.

The two charge functions in (1) and (2) have been interpolated by low order polynomials of orders n_1 and n_2:

$$Q(V_1, V_2) \approx P_{n1}(V_1)\, P_{n2}(V_2).$$

The drain current $I_d(V_1, V_2)$ has been interpolated by a polynomial in the V_1 direction and an Hyperbolic tangent in the V_2 direction, as proposed by Curtice in [16]:

$$I_{ds}(V_1, V_2) \approx P_n(V_1) \quad (a_0 + a_1 V_2) \tanh (a_3 V_2).$$

The orders of all the polynomials P_{n1}, P_{n2}, P_n are such that the error is low and there are no ripples in the data.

B. Small Signal Simulation

To easily check the consistency of the model, a circuit simulation with small signal generator and 50 Ω loads has been performed. Assuming very low ac voltage amplitude, and analyzing the circuit using a harmonic balance algorithm, the S-parameters of the instantaneous model can be computed at any bias point from the ratio of reflected to incident waves at each port. Very few iterations are needed to achieve convergence since the amplitude is small. A comparison is performed between these computed S-parameters at the nominal bias, and the ones measured. As will be shown in Section V, very good agreement between both sets of parameters was found for the two transistors measured (see Figs. 9 and 15).

C. Large Signal Simulation

A program has been developed for analyzing the circuit of Fig. 4 under large signal conditions. This circuit, although very simple, is useful for obtaining valuable data in the design. Since the topology of the model is also very simple, the analysis is very fast, thus allowing to perform an optimization process.

First of all, it has been used to simulate load Pull measurements for obtaining the optimum load impedance for maximum output power. Setting $Z_g = Z_d = Z_0$, the generators produce constant values for $|a_1|$, and $|a_2|$. For a given value of $|a_1|$ (started at small signal), the amplitude and phase of a_2 are varied until the computed output power

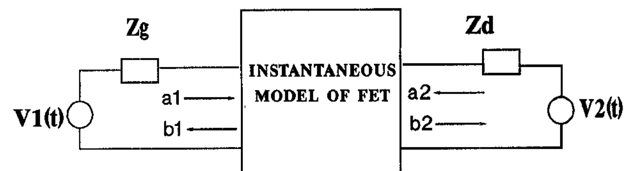


Fig. 4. Circuit for load pull simulation using Harmonic Balance analysis.

is maximum. The optimum load reflexion coeficient is then a_2/b_2. The procedure is repeated for increasing input power levels, giving the evolution of optimum load impedance. Its value for small signal corresponds to the input-output simultaneous conjugate match (if the transistor is stable) which can be computed from the S parameters. This is the starting value in the maximization procedure.

Also the compression characteristics (P_{out} versus P_{in}) of the transistor can be obtained at fundamental and harmonic frequencies for any load condition.

To simulate the transistor in a more specific circuit, such a microstrip amplifier, the model can be introduced on commercial packages, such as HP MDS, as a user model.

V. Experimental Results

All the ac measurements were carried out using an HP8510B network analyzer together with a test fixture developed in our laboratory [17]. This test fixture allows the measurement of S parameters of transistors up to 40 GHz, using a TRL calibration. Two "line" standards were used for allowing measurements to be done in the two frequency bands mentioned in section III.

The dc measurements were performed by means of a computer controlled power supply with a semiautomatic procedure also developed in our laboratory.

The following paragraphs show the results obtained for a low noise MESFET and a power MESFET. Both are in chip form and bonded to alumina microstrip lines using thermocompression. The die attach is made with conductive epoxy.

A. Low Noise Transistor FSX02X

This is a submicron recessed gate low noise MESFET from Fujitsu with 9.5 dB gain at 12 GHz. It has been used as a test bench for our procedure.

Fig. 5 shows the values of the elements of the small signal equivalent circuit (Fig. 2) as function of the measurement frequency (1 to 3 GHz). This is the result of the procedure explained in Section III-B by which a set of values is obtained at each frequency point. Note that, as expected, there is little dependance with frequency. Not shown are G_{gs} G_{gd} and τ because their values were very small, oscillating to positive and negative.

Table I shows the corresponding mean values. For each element two values are displayed, one being the previous result, and the other the final value obtained after opti-

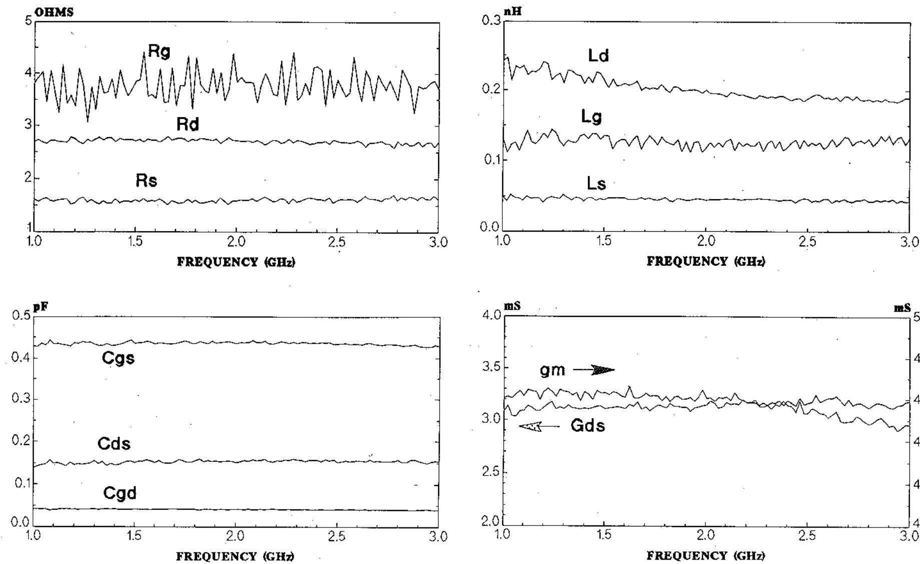


Fig. 5. Values of the elements of the equivalent circuit of transistor FSX02X as obtained at each frequency point.

mization of the circuit from 6 to 40 GHz using the former as initial value.

Fig. 6 shows the comparison between the measured S-parameters at nominal bias point (3 V, 10 mA) and those corresponding to the equivalent circuit before and after optimization. Although the frequency band of measurement (6 to 40 GHz) is different than that of the obtention of the elements (1 to 3 GHz), the agreement is very good.

The 6 to 40 GHz S-parameters were measured at 99 bias points in the range $0 < V < 4$ V, $-2 < V < 0$ V. At each bias point an optimization was performed keeping constant the extrinsic elements, obtaining then the evolution of the intrinsic parameters with the bias voltages. Fig. 7 shows the results. By numerical integration of these curves, the current and capacity functions were obtained, and are shown in Fig. 8. There are no curves for $I_g(V_g, V_d)$ since the corresponding conductances were zero. Note that the $I_d(V_g, V_d)$ function is similar to the dc characteristics of the transistor, but is not identical.

This instantaneous equivalent circuit was used to compute the S parameters of the transistor, analyzing it under small signal condition at the nominal bias point ($V_{ds} = 3$ V $I_d = 10$ mA), using a harmonic balance algorithm (see Section IV-B). The resultant S-parameters are shown in Fig. 9 compared with the measured ones. The fitting is very good, showing that the model can be used in circuit analysis.

Fig. 10 shows the output power at fundamental and first harmonic plotted against the input power at 12 GHz, for a transistor loaded with 50 Ω. Very good agreement is obtained with respect to the measurements performed, thus validating the model for large signal analysis. In Fig. 11 the computed optimum load impedance for maximum output power is plotted as function of the input power at 30 GHz. It has been obtained from the Load Pull simulation using the circuit of Fig. 4. Unfortunately, no Load-Pull test bench was available to validate the results.

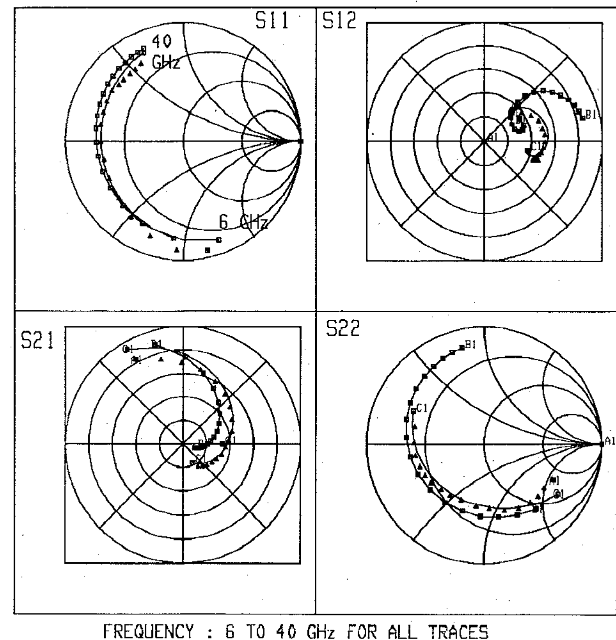
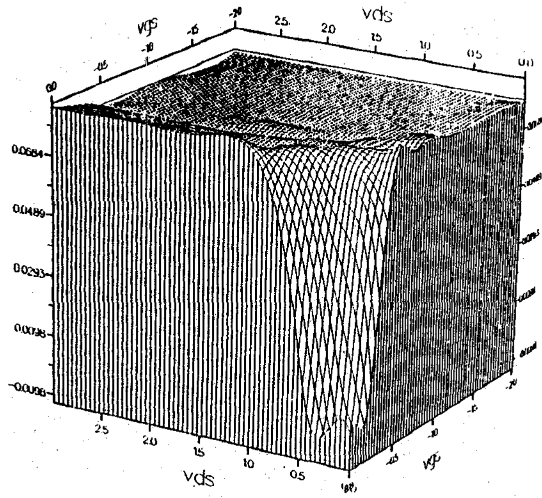


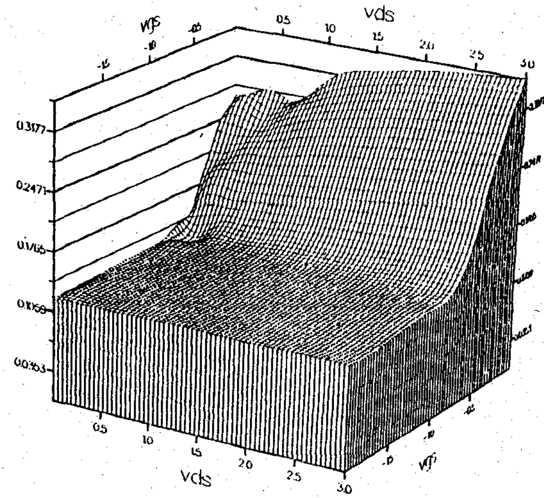
Fig. 6. Comparison between measured and equivalent circuit S-parameters for transistor FSX02X. △: Measured. □--□: Equivalent circuit without optimization. ---: Equivalent circuit after optimization.

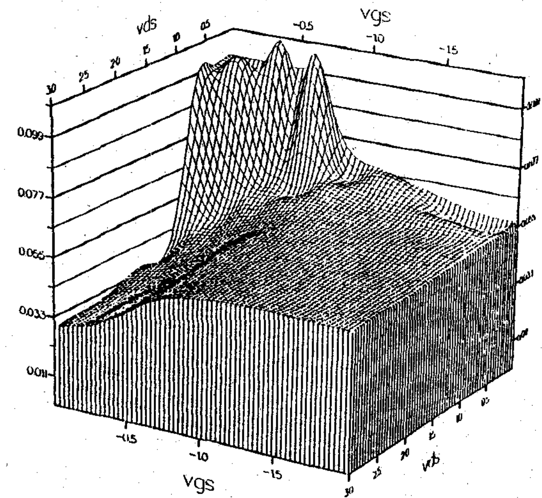
A. Power Transistor JS8864-AS

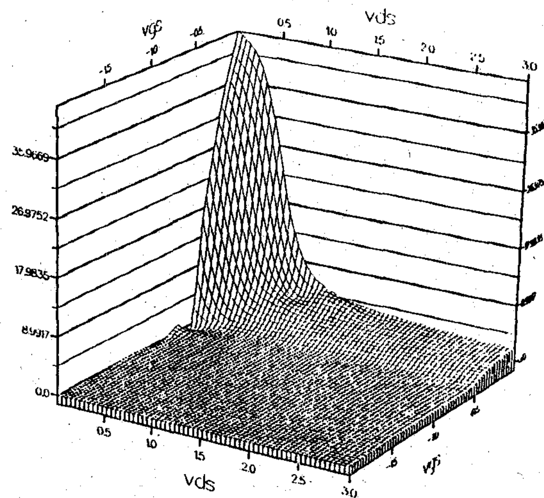
Toshiba's JS8864-AS transistor is a power MESFET capable of delivering 22 dBm output power at 30 GHz. It consists of 6 transistors in parallel with a total gate width of 800 μ (Fig. 12(a)). It was used for the design of a 28 GHz power amplifier for which it was previously modelled. It has no via holes, and the source to ground connection was done using 7 Au wires 0.15 mm long, and 25 micron diameter. Gate and source were connected with 6 wires each, having each one 0.3 mm length. The photograph of Fig. 12(b) shows the assembly.

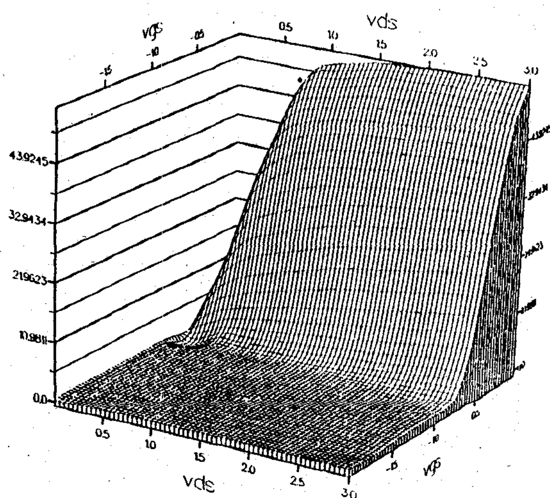
Unexpected problems were found in the extrinsic ele-











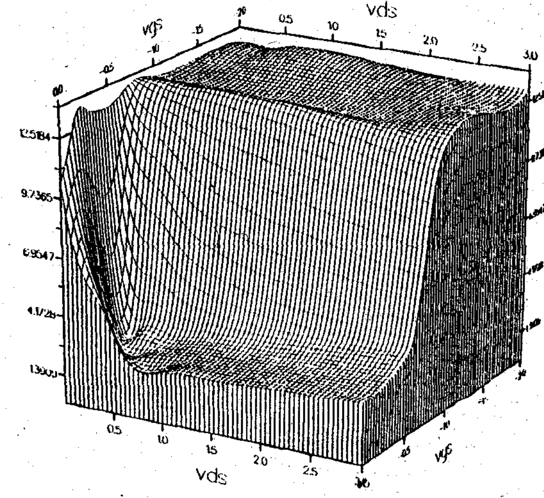


Fig. 7. Elements of the equivalent circuit of FSX02X as function of the bias voltages.

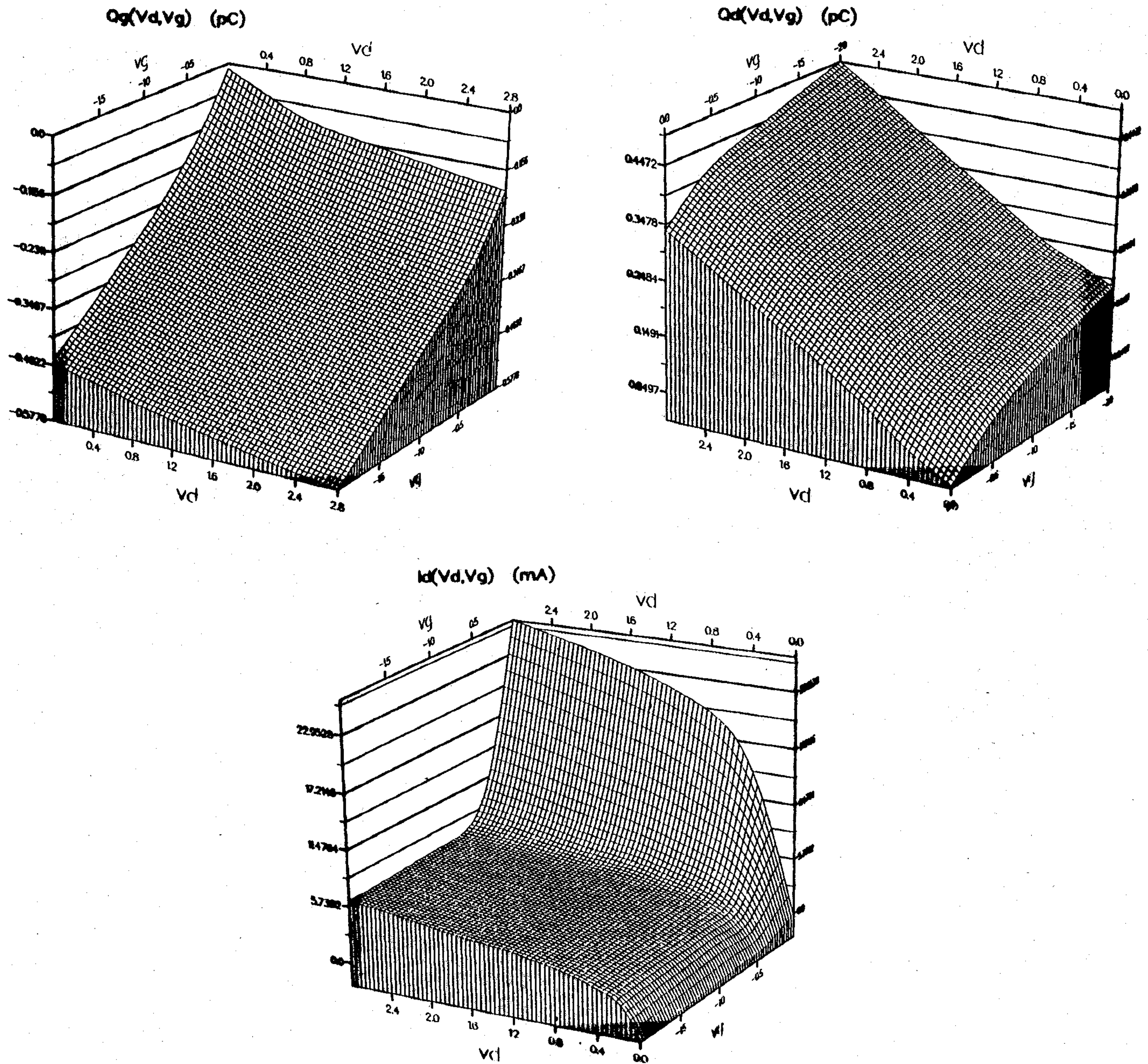


Fig. 8. Instantaneous charge and current functions for FSX02X.

ments measurement of the small signal equivalent circuit using the method of [6]. As explained in Section III, this is based in the assumption of a very simple equivalent circuit of the transistor under positive gate voltage and zero drain bias (Fig. 3). In this model, and for sufficiently high gate currents, the Z-parameters have their real parts constant and their imaginary parts linearly dependent with frequency. The measurements performed for $I_g = 140$ mA (Fig. 13) show a resonant behavior on the imaginary part of Z_{11}. The real part of Z_{11}, however, is still constant with frequency, and linear with $(1/I_g)$, as shown in Fig. 14.

The problem was solved using initially the values supplied by the manufacturer for extrinsic elements, as starting values for the optimization. However, to obtain good results, the entire procedure had to be carried out several times, with different extrinsic elements. This shows the importance of an accurate determination of them.

Fig. 15 shows the comparison between the measured S-parameters and those simulated by harmonic balance analysis. The result is good, but it was highly dependent on the value of the extrinsic elements.

C. Power Amplifier

A 28 GHz power amplifier was designed according to the data provided in the procedure described above. Since the transistor has low gain (about 4 dB at 1 dB compression point) a two stage amplifier was considered. The impedance matching networks were designed on microstrip lines fabricated on alumina substrate ($\epsilon_r = 9$ $h =$

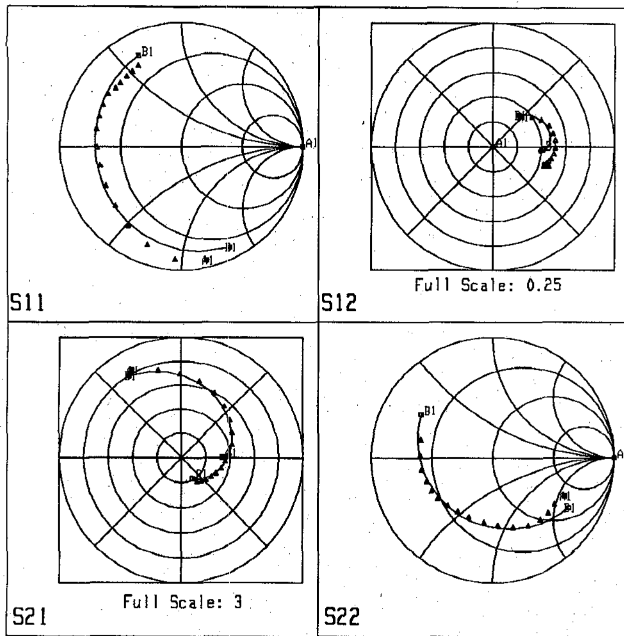


Fig. 9. Comparison between S-parameters measured and simulated from harmonic balance analysis. △: Measured. ---: Simulated.

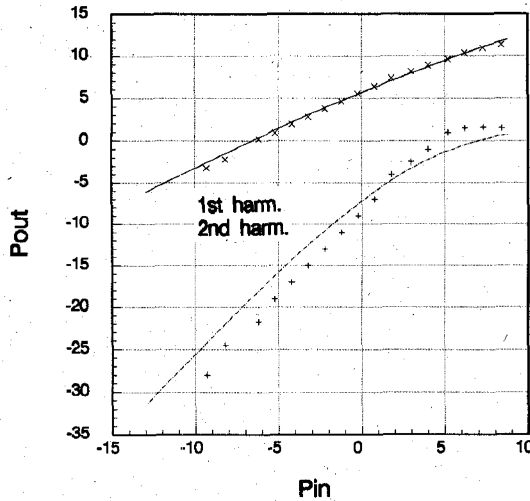


Fig. 10. Output power versus Input power for transistor FSX02X with 50 Ω load at 12 GHz and for 1st and 2nd harmonic. X: Measured. --- Simulated.

0.254 mm), and using a configuration of coupled lines (Fig. 16) to avoid the use of decoupling capacitors, which are difficult to characterize at those frequencies. Input and output interfaces were coaxial OS-50 connectors. Two designs were fabricated, one corresponding to matching for maximum small signal gain, and the other matched for maximum output power, as obtained from load pull simulation. Fig. 17 shows the plot P_{out}-P_{in} for the last one. The curve does not take into account the losses in the matching networks nor in the microstrip to coaxial transition thus the transistor is effectively delivering more than 21.5 dBm in agreement to the data supplied for the manufacturer. This result was obtained without any adjustment and was confirmed by at least 6 identical units fab-

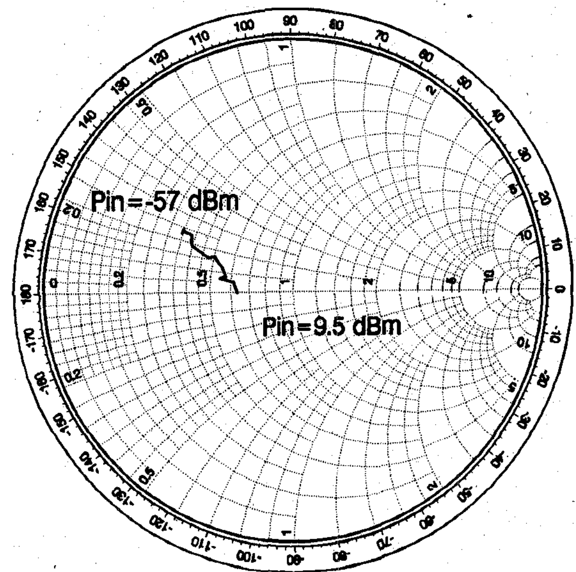
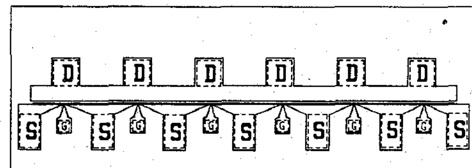
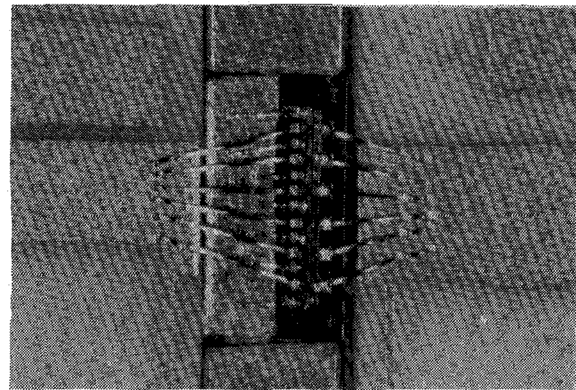


Fig. 11. Output impedance for maximum output power as function of input power for transistor FSX02X at 30 GHz. Obtained from load pull simulation.



(a)



(b)

Fig. 12. Transistor JS8864-AS. (a) Chip outline. (b) Photograph of the assembly.

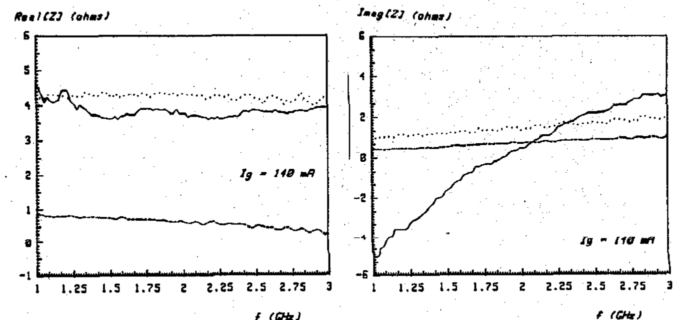


Fig. 13. Z parameters measured (converted from S-parameters) of transistor JS8864-AS for positive gate voltage and zero drain voltage. -- : Z_{11} -·-: Z_{12}, · · · : Z_{22}.

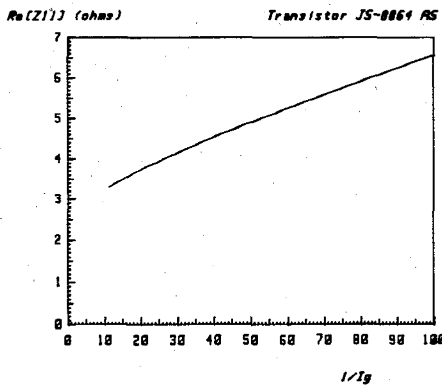


Fig. 14. Real part of Z_{11} for transistor JS8864-AS as function of $1/I_g$.

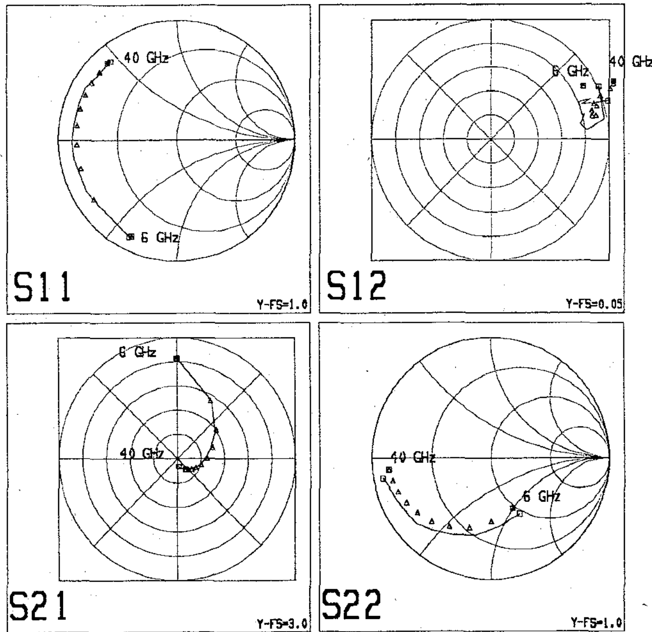


Fig. 15. Comparison between measured and simulated S-parameters of transistor JS8864-AS. --- : Measured, $\triangle$: Simulated from harmonic balance analysis.

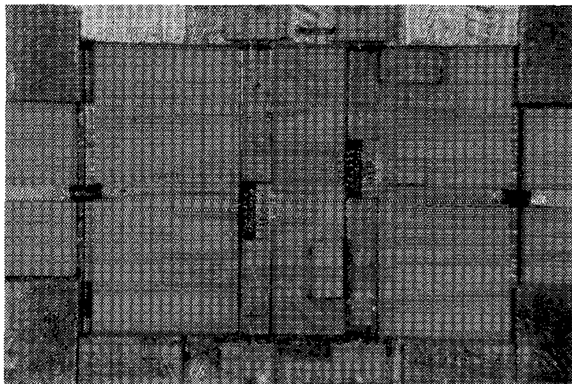


Fig. 16. Photograph of the two-stage 28 GHz power amplifier designed using transistor JS8864-AS.

ricated, for which the same (approximated) characteristics were measured. A higher power amplifier was fabricated from the combination of two such basis amplifiers.

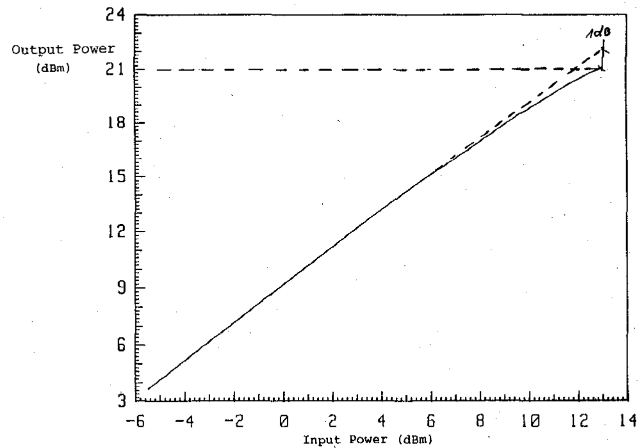


Fig. 17. Output power vs input power measured at 28 GHz for the amplifier of the previous figure.

VI. Conclusion

A new approach for FET modeling have been presented. It consists of instantaneous current and charge generators depending on two voltages. Additionally, the parasitic extrinsic elements are also included. For packaged transistors the parasitics associated to the package have also to be taken into account. The model predicts the FET operation in both small signal and large signal operation and is well suited for nonlinear analysis using harmonic balance. It is obtained from the small signal equivalent circuit in which the intrinsic elements are bias dependent. This small signal circuit results from a parameter extraction procedure based on measured S-parameters. The extrinsic elements are obtained from dc and cold-FET ac measurements, and the intrinsic elements analytically at each frequency point. A further optimization is performed to increase the accuracy of the equivalent circuit.

The instantaneous model has been used in a harmonic balance analysis program to simulate the transistor. The S-parameters simulated in this way agree very well with the measured ones, and also the nonlinear effects such as gain compression and harmonic generation. A load pull simulation for obtaining the load for maximum output power has also been implemented. The procedure has been carried out for two transistors, one being a low noise one and the other a power transistor. The results for both are satisfactory, although problems in the characterization of the power transistor have appeared.

For the power transistor, the results have been used for the design of a microstrip power amplifier at 28 GHz, obtaining output power in excess of 21 dBm at 1 dB compression point.

Acknowledgment

Most of the results for the extrinsic elements of the equivalent circuit are based on unpublished work and helpful discussions of Professor Eduardo Artal, to whom the authors are indebted. The experimental work, espe-

the power amplifier, was successful thanks to the fine work of A. Cano in the mechanical shop and J. Giner in the assembling. The authors wish to thank also J. Mª Haro for his work in software maintenance. The microstrip lines were fabricated by ENSA.

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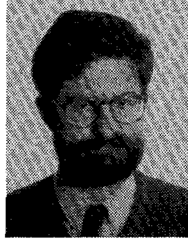

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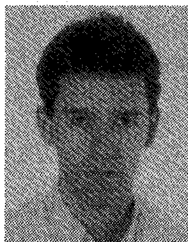

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